U.S.S.N. 09/822,532

REMARKS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

Claims 1-20 are pending in the application. Claims 1-20 stand rejected.

Claim Rejections Under 35 USC §103

Claims 1-20 are rejected under 35 USC §103(a) as being unpatentable over Chakravorty '569 in view of Lin '916 and further in view of Wolf et al publication. It is contended that Chakravorty substantially discloses the invention except a method for removing the insulating material by a wet etching process, and such is disclosed by Lin.

The rejection of claims 1-20 and under 35 USC §103(a) based on Chakravorty, Lin and Wolf et al is respectfully traversed.

Chakravorty discloses a low cost chip size package wherein a plurality of metal bumps is formed on a semiconductor wafer containing a plurality of chips, each of the plurality of bumps is in electrical contact with a contact pad on one of the

chips. Chakravorty further discloses the deposition of an encapsulant layer over the plurality of metal bumps and then polished to expose a top surface on each of the metal bumps. While the Applicant agrees with the Examiner that Chakravorty does not teach a method for removing the insulating material by a wet etching process, the Applicant must respectfully submit that Chakravorty further does not teach the deposition of the insulating material layer to a specific thickness, i.e. **a thickness that is substantially the thickness of aluminum bumps to be formed.**

Furthermore, while Lin discloses the etching of a polyimide layer to an angle of about 75°, Lin does not disclose the removal of "at least partially" a thickness of the insulating material layer. As clearly recited in the present invention independent claim 1:

> "Claim 1. A method for forming aluminum bumps by sputtering and chemical mechanical polishing comprising the steps of:
>
> providing a pre-processed electronic substrate ...;
>
> depositing an insulating material layer on top of said plurality of I/O pads to a thickness

that is substantially the thickness of Al bumps to be formed;

photolithographically forming a plurality of openings ...;

sputter depositing a metal comprising Al ...;

chemical mechanical polishing said electronic substrate ...; and

removing at least partially a thickness of said insulating material layer by a wet etch process."

Furthermore, in the present invention independent claim 12:

"Claim 12. A method for forming aluminum bumps on a semiconductor structure comprising the steps of:

providing a pre-processed semiconductor structure ...;

printing a layer of polyimide-containing material having a thickness of at least 5 μm on top of said structure;

forming a plurality of openings ...;

filling said plurality of openings ...;

removing excess metal from areas ...; and

removing at least partially said layer of polyimide-containing material by a wet etch process."

The Applicant respectfully submits that the art cited by the Examiner, i.e. Chakravorty, Lin and Wolf et al, even when combined, do not teach the present invention process steps of

"depositing an insulating material layer to a thickness that is substantially the thickness of aluminum bumps" (claim 1),

"printing a layer of polyimide-containing material having a thickness of at least 5 μm on top of said structure" (claim 12), and

"removing at least partially a thickness of said insulating material layer" (claims 1 and 12).

In the Response to Arguments section of the 04/17/2003 Office Action, the Examiner stated "Applicant's argument concerning the thickness of the insulating material is noted. However, the Lin reference does teach that the insulating layer be about the same thickness of the bump. Also, the reference clearly, shows a polyimide layer thicker than 5μm as claimed". Throughout the Lin reference, the Applicant failed to find any support to substantiate the Examiner's statement. Lin teaches a method in which a polyimide polymer is used as an inter-metal dielectric layer (see Abstract) and then, as shown in Figure 8, a via 70 is etched in the polyimide layer 64 (col. 7, lines 42-48). The Lin reference has nothing to do with the building of solder bumps, or anything to do with the present invention in which a polyimide layer is used as a mold for molding solder bumps.

The Examiner further stated that "the Chakravorty reference does teach col. 11, that by using an etch method to control exposure at the bumps, which includes thinning the insulation material as claimed".

The Applicant respectfully submits that Chakravorty stated at col. 11, lines 1-18:

> "The next step consists of exposing the metal bump regions 311 by removing the portions of encapsulant layer 312 which cover bumps 311. In one embodiment, that is achieved by **mechanically polishing** the encapsulated wafer in a polishing wheel with the slurry such as alumina. ... methodologies established in the area of chemical-mechanical polishing (CMP) could also be employed for a controlled process for exposure of the metal bump regions 313."

The Applicant failed to find any teaching by Chakravorty of using an etch method to remove the insulating material layer, let alone the teaching of the present invention of "removing at least partially a thickness of said insulating material layer by a wet etch process".

The rejection of claims 1-20 under 35 USC §103(a) based on Chakravorty, Lin and Wolf et al is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

U.S.S.N. 09/822,532

Based on the foregoing, the Applicant respectfully submits that all of the pending claims, i.e. claims 1-20, are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicant's representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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